Karlsruhe Institute of Technology

Hoch- und Höchstfrequenzhalbleiterschaltungen (HHHS)
Millimetre-wave monolithic integrated circuit design

Winter term 2013/2014

Frequency Multiplier

INSTITUT FÜR HOCHFREQUENZTECHNIK UND ELEKTRONIK

KIT – University of the State of Baden-Wuerttemberg and
National Research Center of the Helmholtz Association

lecture outline

- applications and figures of merit
- diode multipliers
  - current multipliers
- FET multipliers
  - class A FET multipliers
  - class B/C FET multipliers
  - balanced FET doublers
- multiplier theory
  - effect on phase and amplitude modulated signals
  - harmonic terminations
- practical example

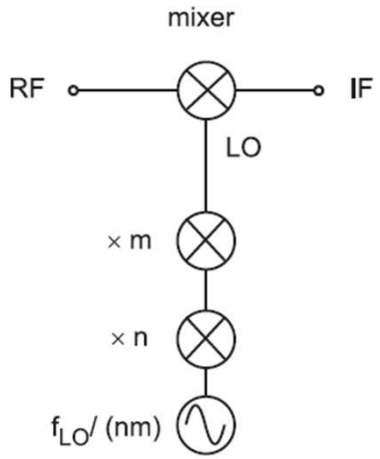
frequency translating circuits

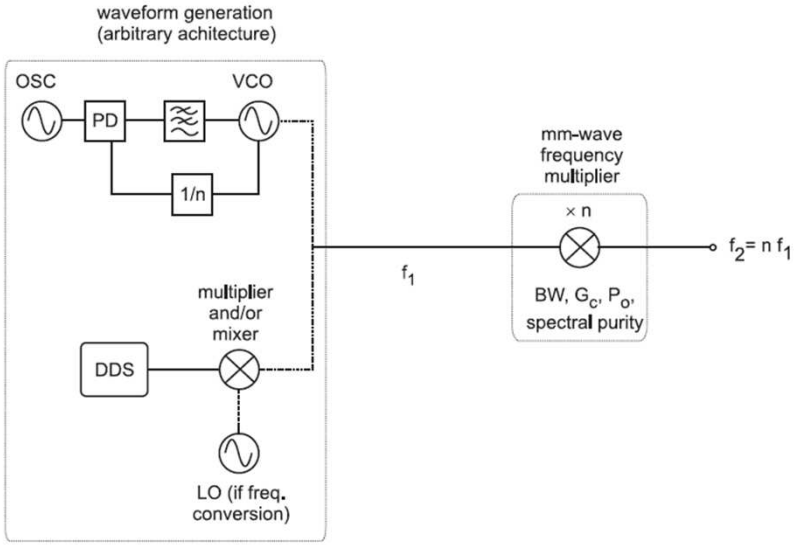
- This part of the lecture is based on the lecture “Active integrated circuits for millimetre wave applications (AICMMA)”, which was given by Prof. Ingmar Kallfass, who is now with the University of Stuttgart.

function	input frequency	output frequency
amplifier	f_0	f_0
harmonic generator	f_0	$i * f_0$, i = 1, 2, …
frequency multiplier	f_0	$n * f_0$
(fundamental) mixer	f_0	f_{LO} +/- f_0
subharmonic mixer	f_0	$n * f_{LO}$ +/- f_0

multiplier applications

- frequency multiplier as signal source…
  - for transmit signal
  - for LO signal
- advantages
  - high absolute bandwidths possible
  - higher output frequencies than oscillators are possible
  - fast frequency tuning (compared to PLL)
  - if monolithic integration, only one high frequency port (RF), none if on-chip antenna
- disadvantages
  - degradation of phase noise
  - creation of unwanted harmonics





multiplier specifications

	entity	symbol	unit	comment
conversion	conv. gain	G_C	dB	if active
	conv. efficiency		%	if passive
	input power	$P_{in,1}$	dBm	
output	bandwidth (rel)	b	%	$b_{in} = b_{out}$
	bandwidth (abs)	B	GHz	$B_{out} = n * B_{in}$
	output power	$P_{out,n}$	dBm	
spectral purity	harm. suppression		dBc	
	phase noise		dBc	+20 log (n)
matching	input		dB	
	output		dB	

multiplier classification

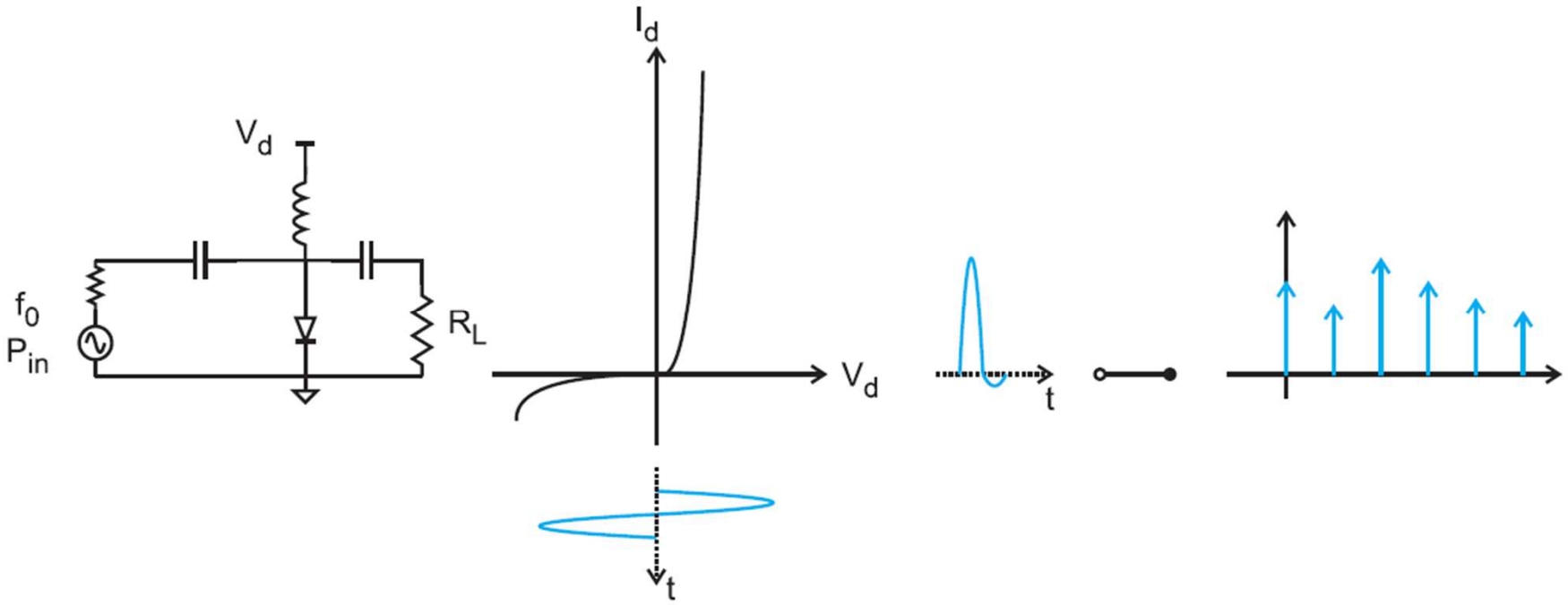
- nonlinear device
  - diode: I_d (V_d), C_d (V_d)
  - transistor: I_{ds} (V_{gs},V_{ds})

- topologies
  - series- or parallel connection of nonlinear element
  - balanced topology
  - anti-parallel diodes

nonlinear entity	passive	active
real	Schottky diodes	FET, HBT
reactive	varactor diodes	

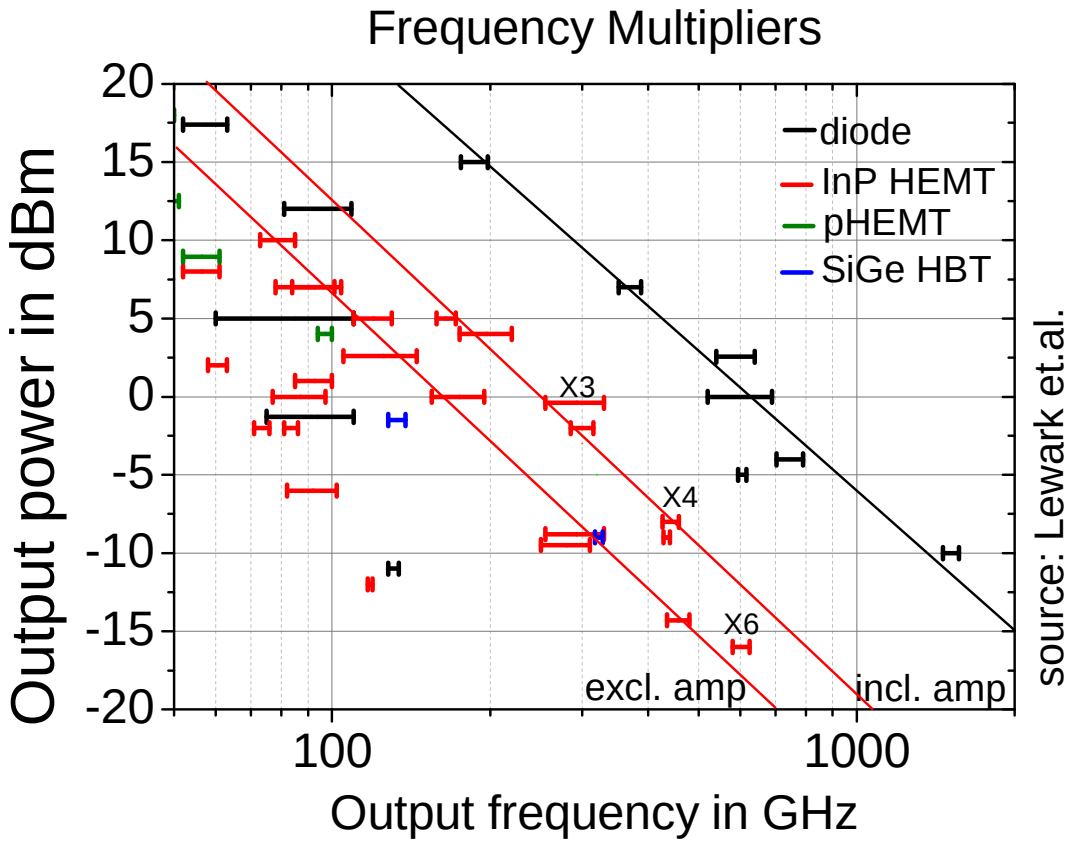
exploiting nonlinear transfer characteristics

- harmonic generators require transfer characteristics with...
  - no symmetry
    - single diode
    - class-B,C FET



multiplier state-of-the-art

- diode
  - no integration possible
  - low efficiency
  - relatively inexpensive
  - robust



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  - current multipliers

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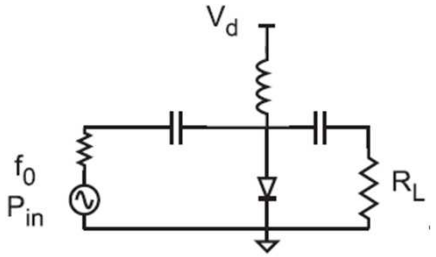
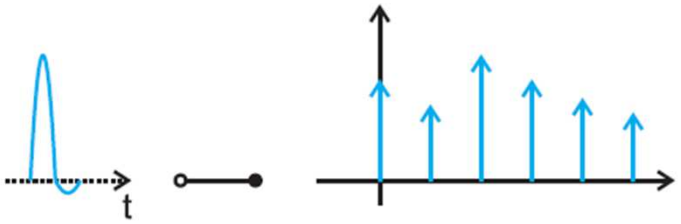
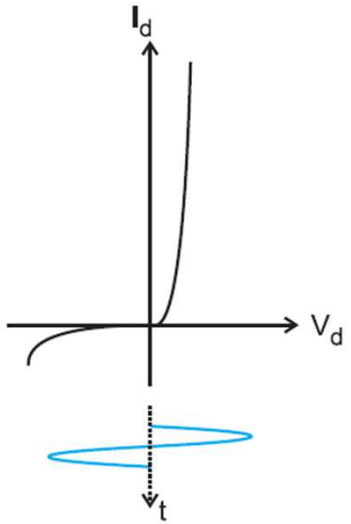
current multipliers
single-ended diode multiplier

- exploit nonlinear current
  - $I = I_s\left(e^{\frac{qV}{kT_a}} - 1\right) = I_s\left(e^{\frac{V}{V_t}} - 1\right)$
- generation of harmonics
  - all harmonics present
  - $V = \hat{v}_1 \cos\omega_1 t$
  - Taylor series: $e^x = \sum_0^\infty \frac{x^n}{n!} = 1 + x + \frac{x^2}{2} \ldots$
  - $I = I_s\left(\hat{v}\cos\omega_1 t + \frac{\hat{v}^2}{2}\cos^2\omega_1 t + \frac{\hat{v}^3}{6}\cos^3\omega_1 t + \ldots\right), \hat{v} = \frac{\hat{v}_1}{V_t}$
  - $I = I_s\left(\hat{v}\cos\omega_1 t + \frac{\hat{v}^2}{2}\frac{1}{2}(1 + \cos 2\omega_1 t) + \frac{\hat{v}^3}{6}\frac{1}{4}(3\cos\omega_1 t + \cos 3\omega_1 t)\ldots\right)$

- I_s...diode saturation current
- q...electron charge
- k...Boltzmann constant
- T_a...absolute temperature / K
- $V_t = \frac{kT_a}{q}$...thermal voltage







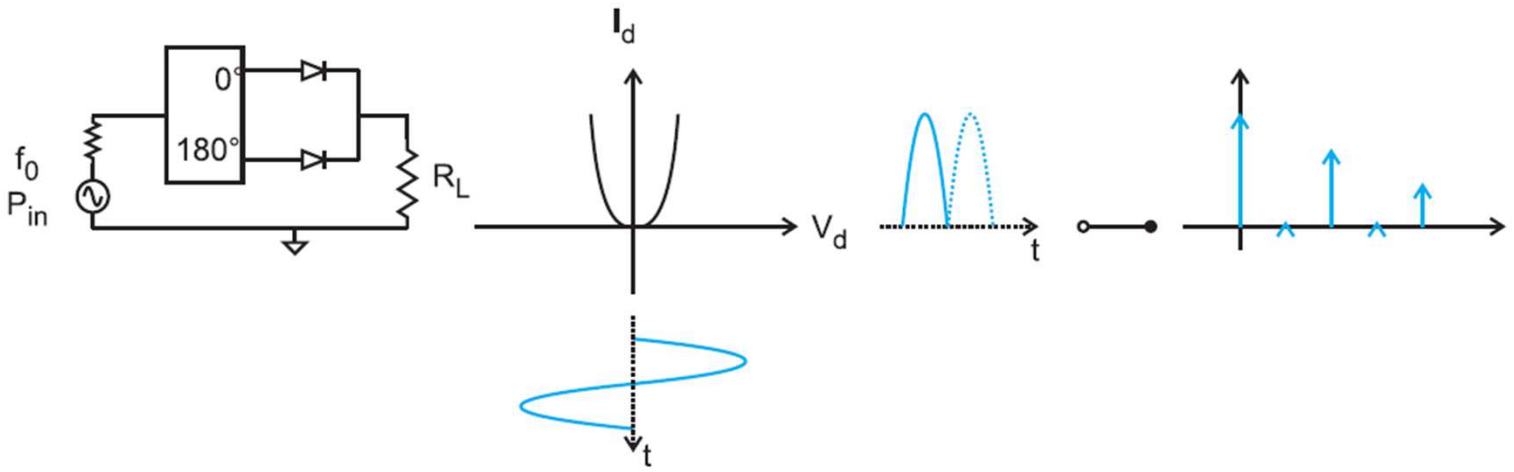
current multipliers
balanced diode multiplier

- exploit nonlinear current

$$I = I_1 + I_2 = I_s\left(e^{\frac{V}{V_t}} - 1\right) + I_s\left(e^{-\frac{V}{V_t}} - 1\right) = I_s\left(e^{\frac{V}{V_t}} + e^{-\frac{V}{V_t}} - 2\right) = 2I_s\left(\cosh\frac{V}{V_t} - 1\right)$$

- generation of harmonics
  - only DC term and even harmonics present

  - $V = \hat{v}_1 \cos\omega_1 t$
  - Taylor series: $\cosh x = \sum_0^\infty \frac{x^{2n}}{(2n)!} = 1 + \frac{x^2}{2!} + \frac{x^4}{4!} \ldots$



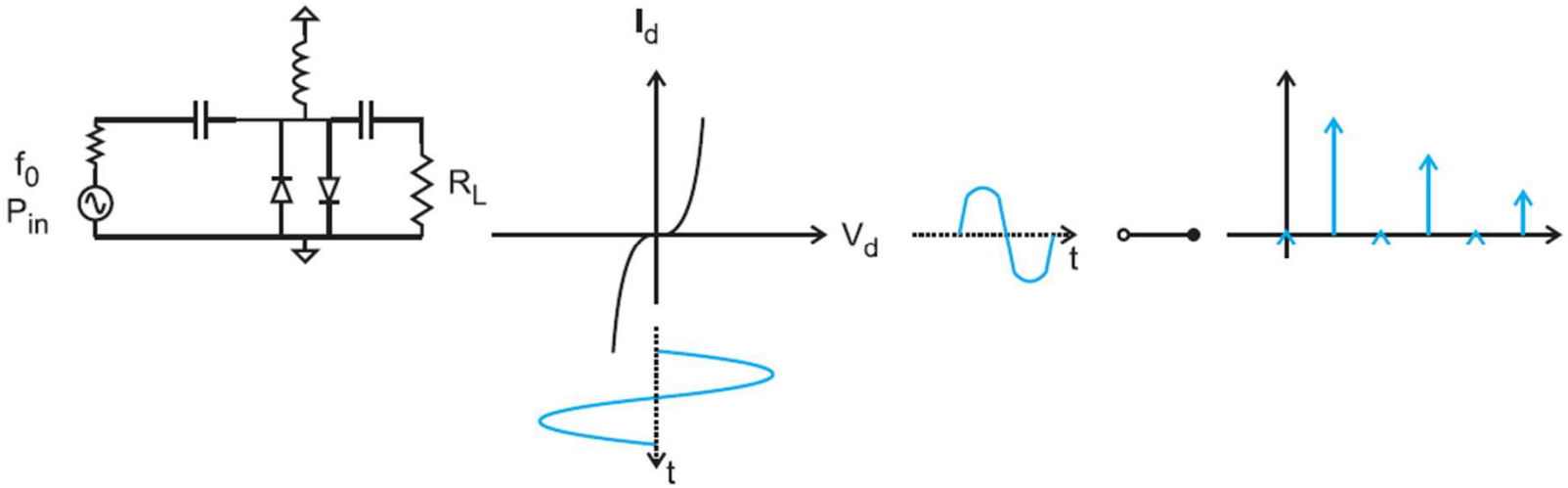
current multipliers
anti-parallel diode multiplier

- exploit nonlinear current

$$I = I_1 + I_2 = I_s\left(e^{\frac{V}{V_t}} - 1\right) - I_s\left(e^{-\frac{V}{V_t}} - 1\right) = I_s\left(e^{\frac{V}{V_t}} - e^{-\frac{V}{V_t}}\right) = 2I_s \sinh\frac{V}{V_t}$$

- generation of harmonics
  - only odd harmonics present

  - $V = \hat{v}_1 \cos\omega_1 t$
  - Taylor series: $\sinh x = \sum_0^\infty \frac{x^{2n+1}}{(2n+1)!} = x + \frac{x^3}{3!} + \frac{x^5}{5!} \ldots$



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class-A FET multiplier

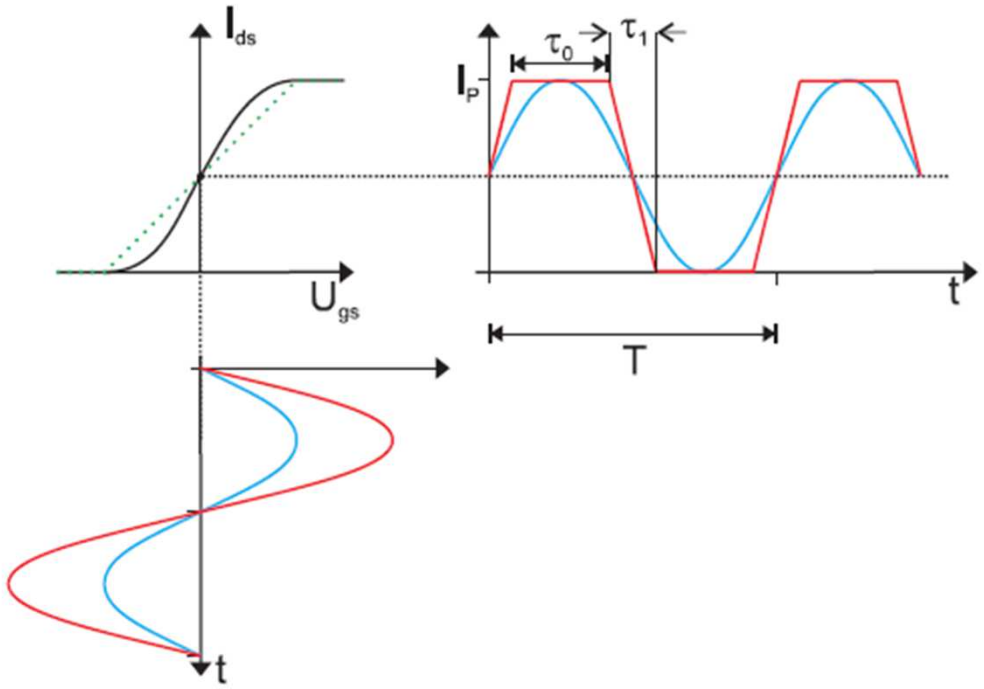
- small input signal → no harmonics at output
- large input signal → symmetrical trapezoidal pulse train at output

- input signal

$$V_{gs} = V_0 + \hat{v}_1 \cos \omega_1 t$$

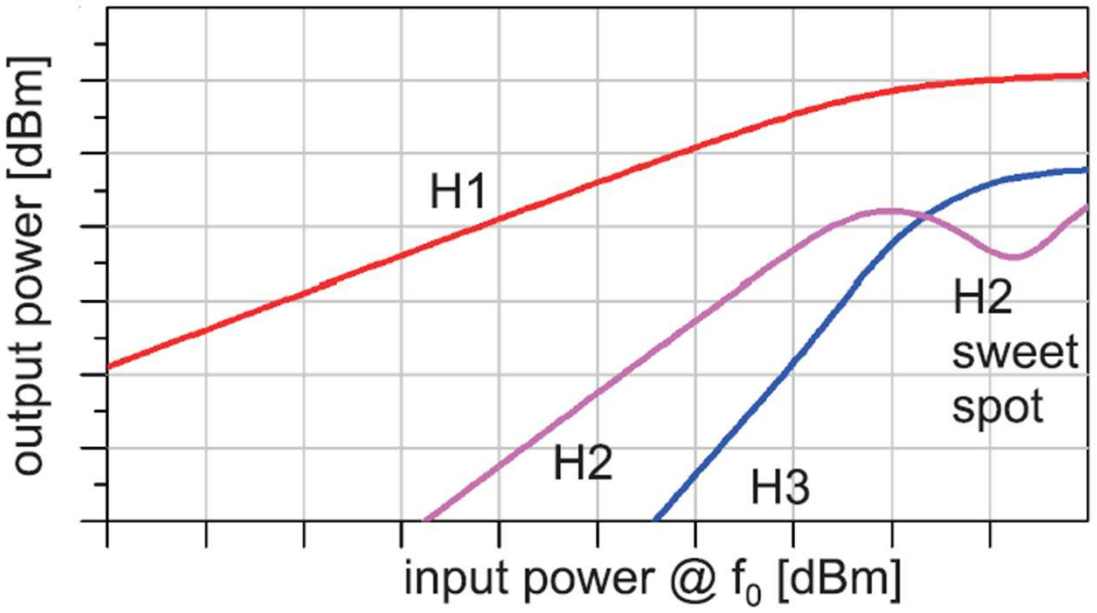
- Fourier Series → generation of harmonics at output
  - ideal case: only odd harmonics present

$$I(t) = (I_{d0} + I_{d1} \sin(\alpha_1) \sin(\omega t) + I_{d3} \sin(\alpha_3) \sin(3\omega t) + I_{d5} \sin(\alpha_5) \sin(5\omega t) + \cdots)$$



class-A FET multiplier

- symmetrical compression
- harmonics versus input power
  - choose appropriate compression level for wanted harmonic
  - “sweet spots” for even harmonics
  - employ differential amplifier with common (& even)-mode rejection



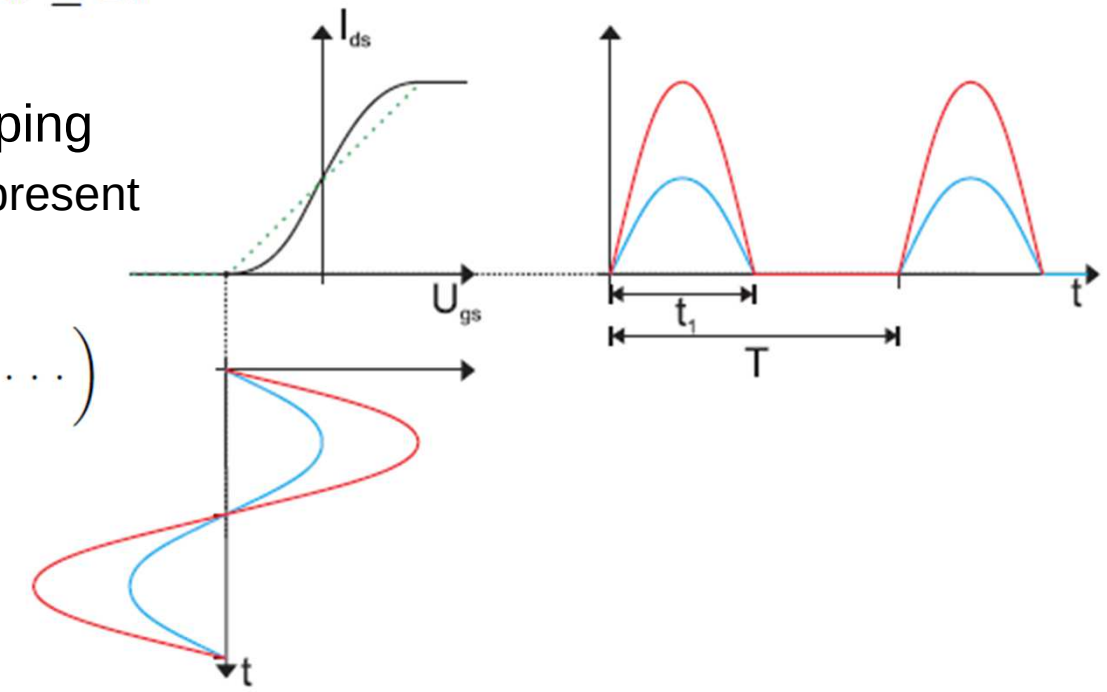
class B/C FET multiplier

- no large signal input required AND class B/C → efficient
- input signal $V_{gs} = V_0 + \hat{v}_1 \cos \omega_1 t$
- output asymmetrically clipped

$$y = \sin x \text{ für } 0 \leq x \leq \pi$$
$$y = 0 \text{ für } \pi \leq x \leq 2\pi$$

- Fourier series at asymmetrical clipping
  - ideal case: only even harmonics present

$$y = \frac{1}{\pi} + \frac{1}{2}\sin x - \frac{2}{\pi}\left(\frac{\cos 2x}{1 \cdot 3} + \frac{\cos 4x}{3 \cdot 5} + \frac{\cos 6x}{5 \cdot 7} + \cdots\right)$$



class B/C FET multiplier

- harmonic contributions versus conduction angle
  - left: linear approximation
  - right: square-law approximation

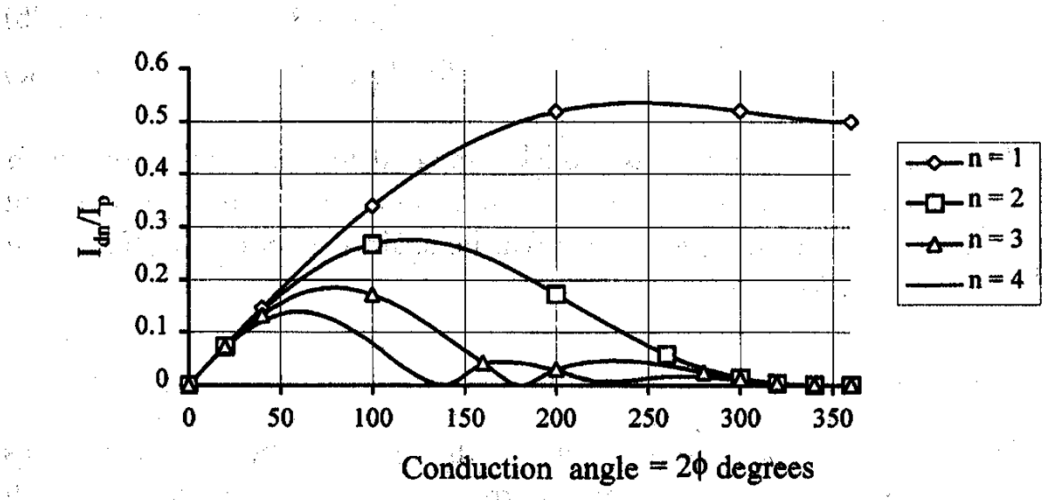


Figure 3.7 Normalized harmonic current as a function of conduction angle.

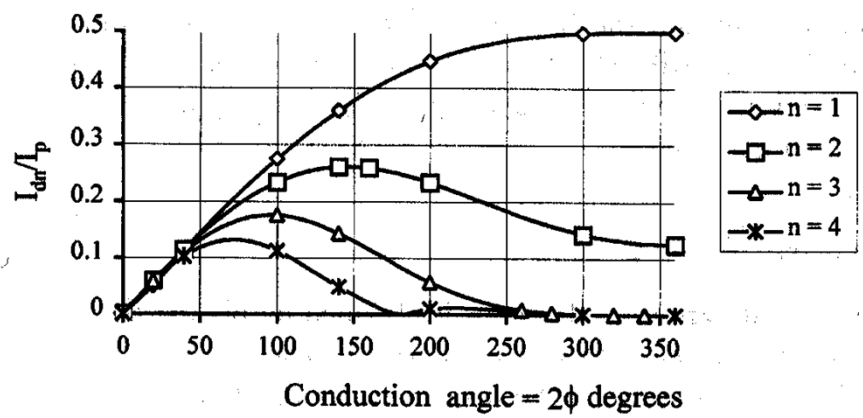
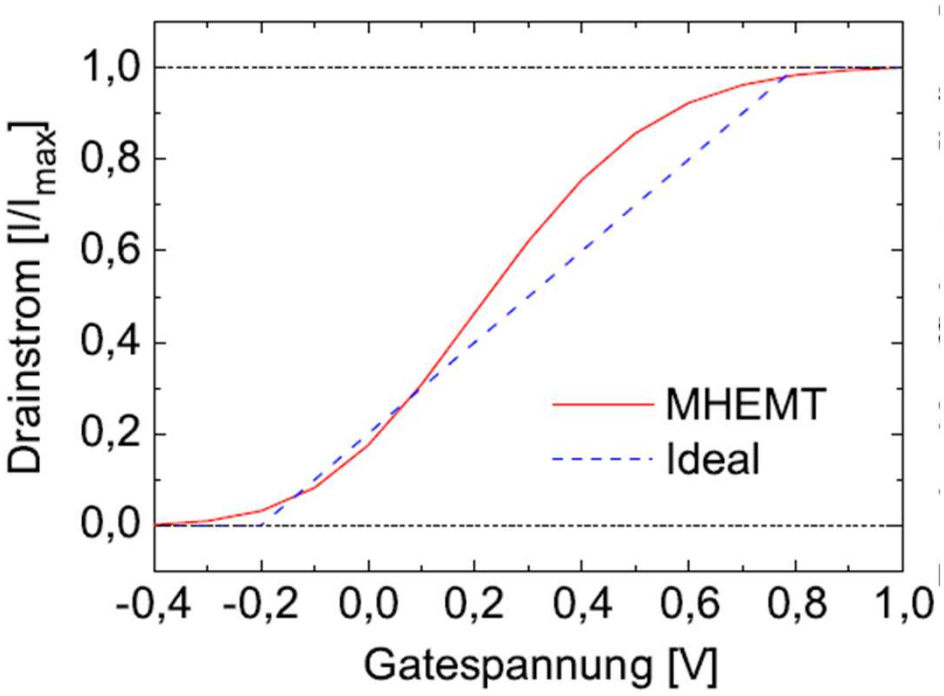


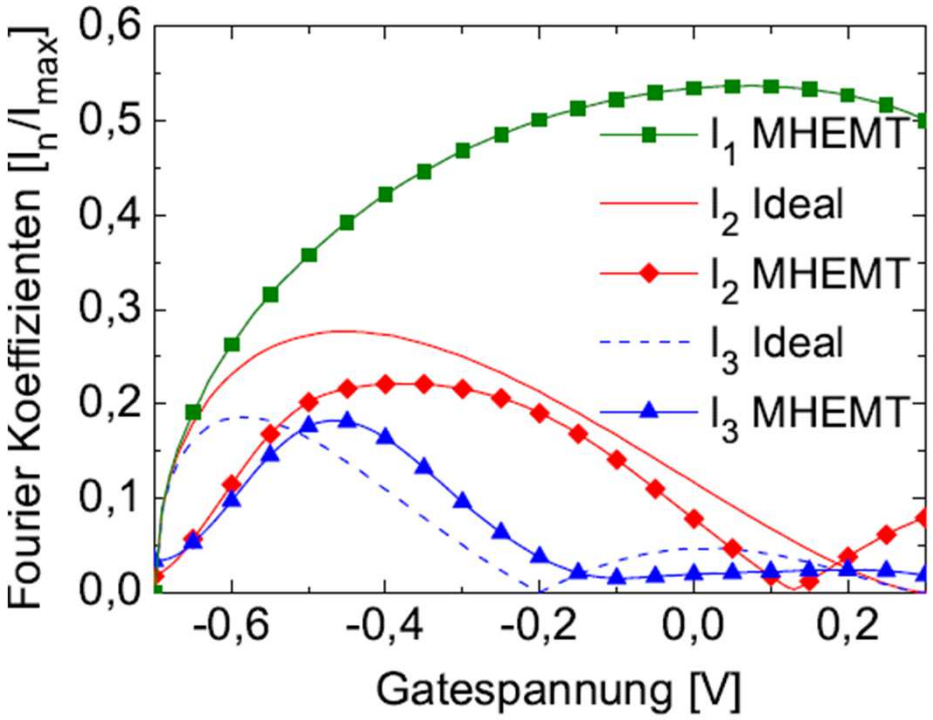
Figure 3.9 Normalized harmonic current as a function of conduction angle.

Source: E. Camargo, “Design of FET frequency multipliers and harmonic oscillators”

example: class B/C FET multiplier

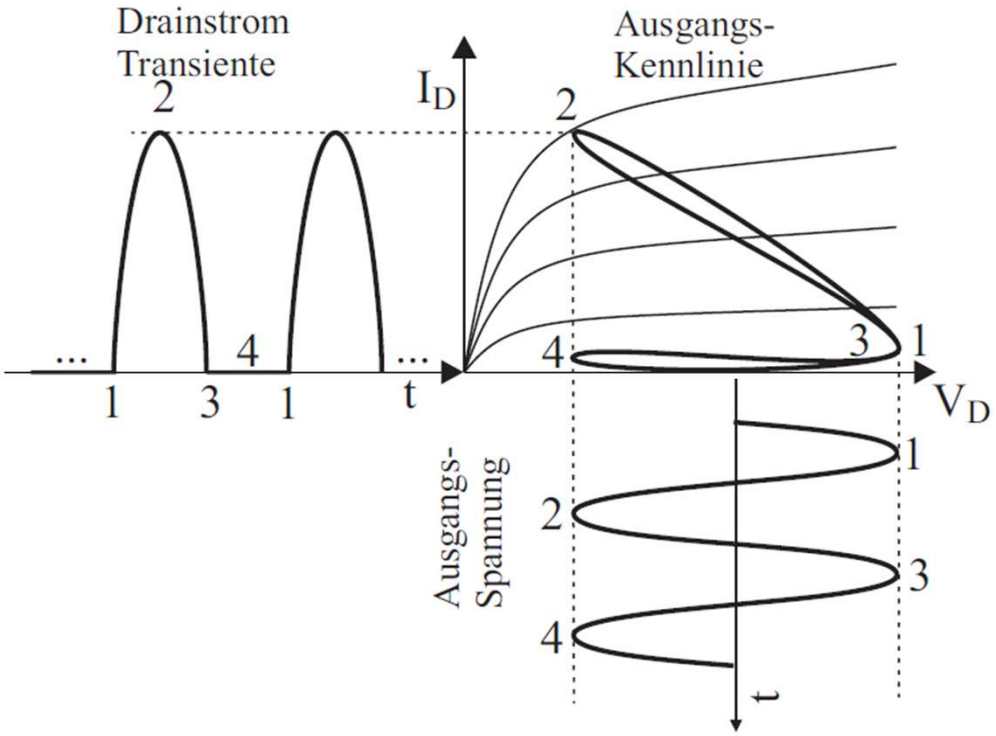
- class B/C bias using an IAF mHEMT transistor
  - 2x30 µm gate width
  - 0 dBm input power
  - sweep of gate bias





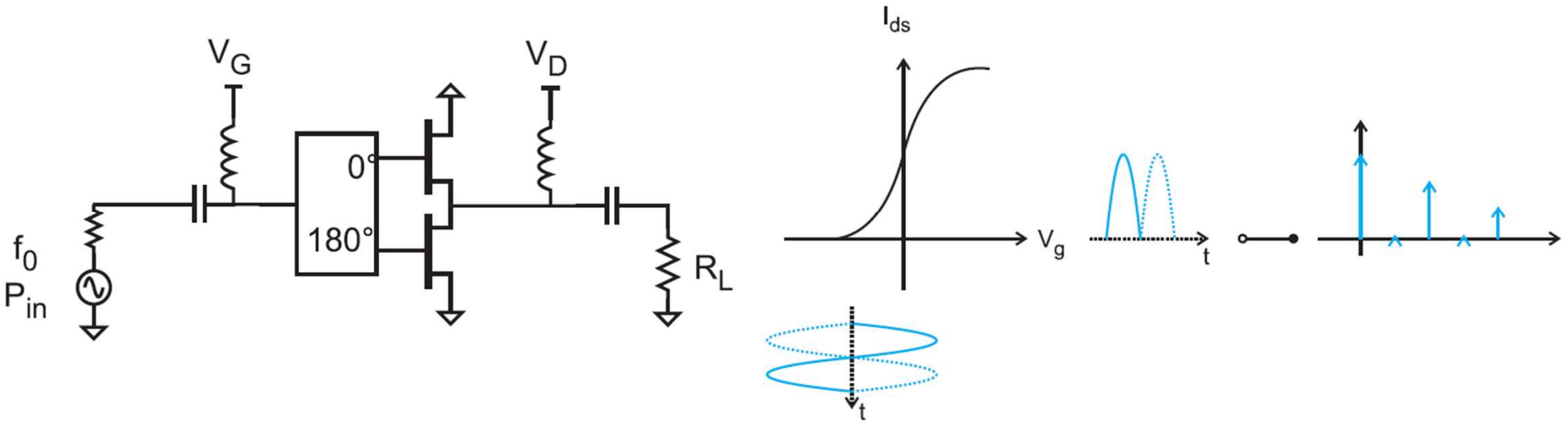
example: single-ended FET doubler

- dynamic IV of a single-ended FET doubler
  - FET biased under class B conditions ($V_G \approx V_{th}$)
  - input match for ω_0 and rejection of higher order harmonics, e.g. low-pass
  - output match for 2 ω_0 and rejection of fundamental frequency
    - e.g. Suppression of fundamental (+ higher even orders) via open ended λ /4 stub



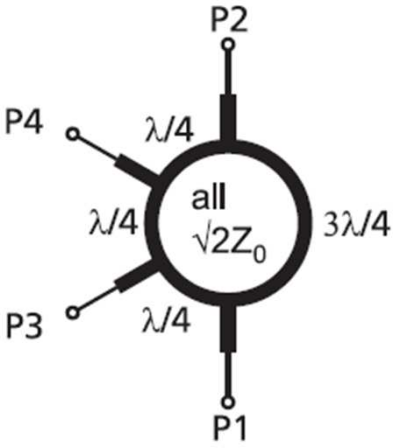
balanced FET doublers

- topology
  - balanced input: passive or active UNBAL
  - FET biased under class B conditions ($V_G \approx V_{th}$)
- harmonics
  - inherent <u>suppression of odd-order</u> (incl. fundamental) harmonics

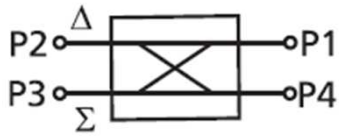


passive 180° Couplers

- Rat-Race
  - isolation of ports P1-P4 and P2-P3 (symmetry)
  - sum (P3) and difference (P2) ports, if input at P1 and P4
  - dimensioning of $Z_L = \sqrt{2}Z_0$: port match

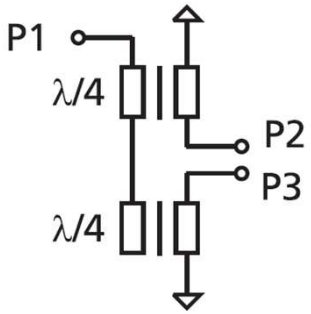


$$S = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & -1 & 1 & 0 \\ -1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix}$$



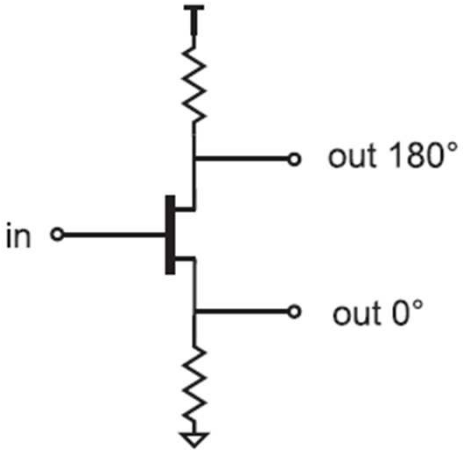
- Marchand-BALUN
  - unbalanced (single-ended, P1) to balanced (differential, P2-3) transformer (UNBAL)

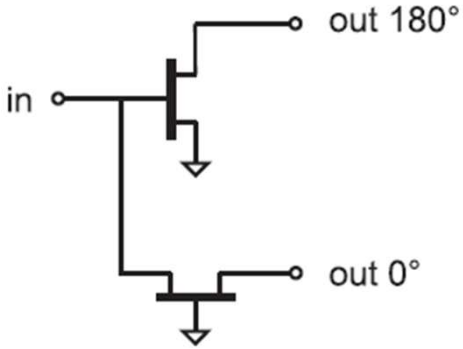
$$S = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & -1 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \end{bmatrix}$$



active BALUN: alternative topologies

- active UNBAL topologies
  - CS: extraction at drain and source
  - CS and CG device
  - shown: RF-only schematics, they omit
    - biasing circuits
    - DC de-coupling
    - impedance matching
- general notes on active UNBALs
  - potentially more compact and broadband than passive λ/4 couplers
  - nonlinear
  - uni-directional
  - DC power consumption





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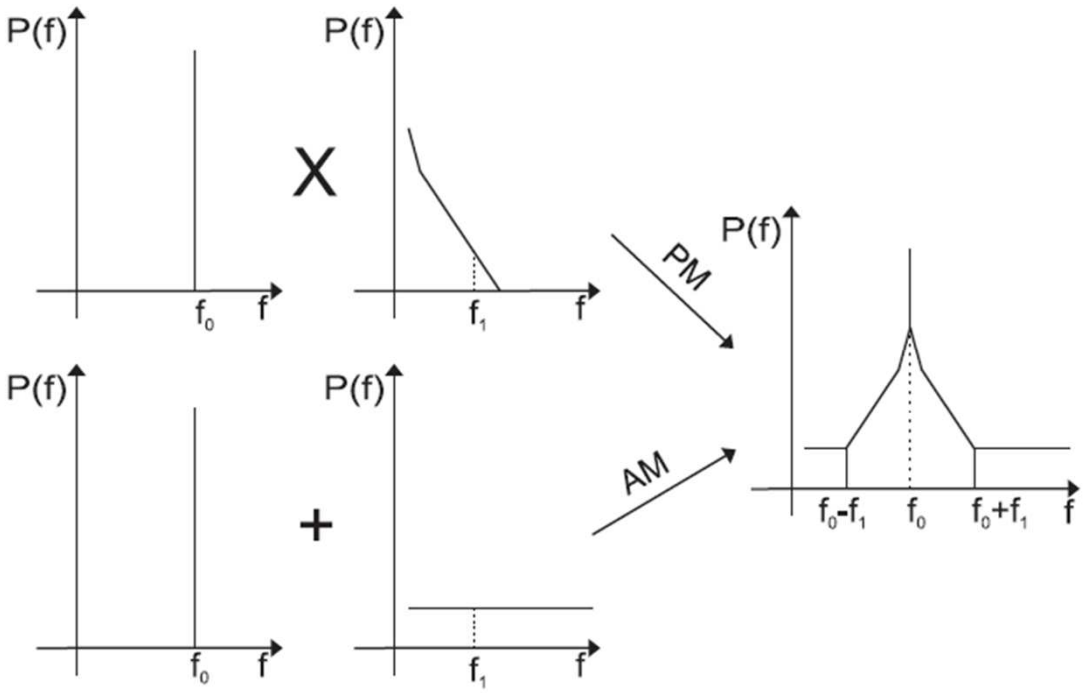
noise contributions

- ideal signal

$$V = \hat{v}_1 \cos(\omega_1 t)$$

- real signal
  - amplitude modulation m(t)
  - phase modulation Φ(t)

$$V(t) = \hat{v}_1 (1 + m(t)) \cos(\omega_0 t + \Phi(t))$$



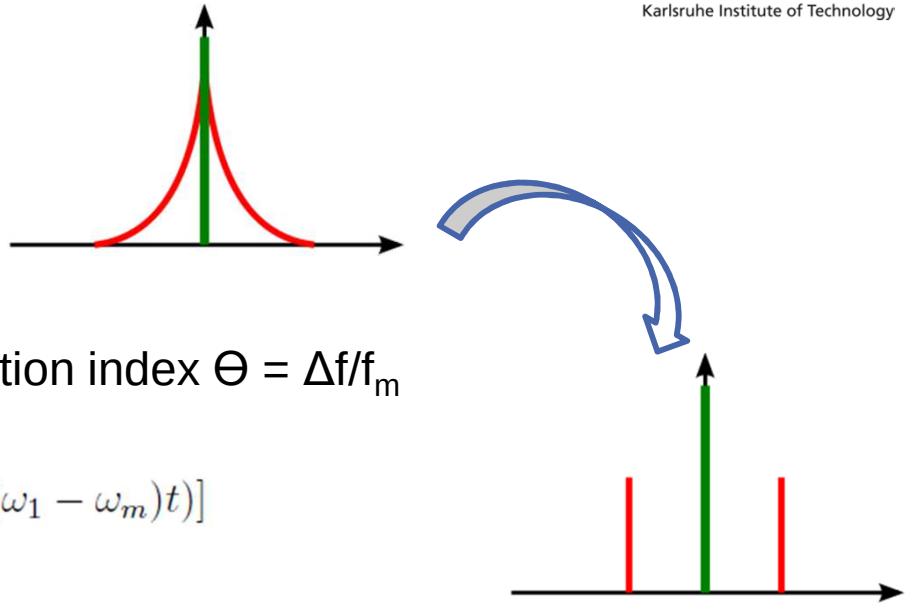
amplitude modulated signal

- modulation index remains unchanged by frequency multiplication
  - before: $v_1(t) = \hat{v}_1 (1 + m(t)) \cos \omega_1 t$
  - after: $v_2(t) = \hat{v}_1 (1 + m(t)) \cos n\omega_1 t = \hat{v}_1 (1 + m(t)) \cos \omega_2 t$

phase modulated signal

- before (1)

$$v_1(t) = \hat{v}_1 \cos(\omega_0 t + \Phi(t))$$



- before (2)
  - frequency modulation with f_m and modulation index $\Theta = \Delta f / f_m$

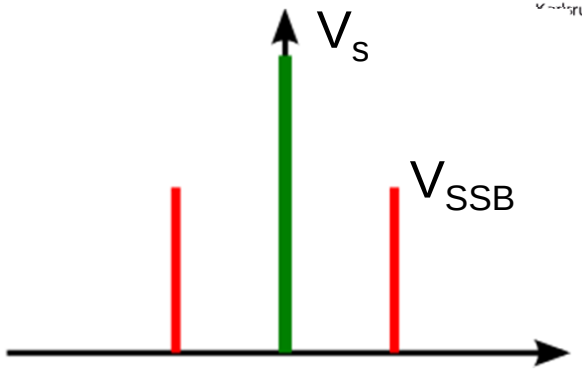
$$v_1(t) = \hat{v}_1 \cos(\omega_1 t) + \hat{v}_1 \frac{\theta}{2}[\cos((\omega_1 + \omega_m)t) - \cos((\omega_1 - \omega_m)t)]$$

- frequency multiplication by n
  - change in modulation index: $\Theta_{new} = n\Theta$ → increase of noise amplitude
  - no change in noise – carrier offset carrier frequency f_m

- $f_2(t) = n f_1(1) = \frac{1}{2\pi}(n\omega_1 + n\omega_m \theta \cos \omega_m t) = \frac{1}{2\pi}(\omega_2 + n\omega_m \theta \cos \omega_m t)$
- phase: $\Phi_2 = \int \omega_2 dt = \int (\omega_2 + n\omega_m \theta \cos \omega_m t)\, dt = \omega_2 t + n\theta \sin \omega_m t$
- signal: $v_2(t) = a_1 \cos(\omega_2 t + n\theta \sin \omega_m t)$

effect on phase noise

- SNR
  - noise amplitude V_{SSB}
  - signal amplitude V_s



$$\mathrm{SNR}_{\mathrm{dB}} = 10\log\left(\frac{V_s}{V_{SSB}}\right)^2 = 20\log\left(\frac{2}{\theta}\right) = 6\mathrm{dB} - 20\log(\theta)$$

- noise degradation

$$\left(\frac{\mathrm{SNR}_f}{\mathrm{SNR}_{Nf}}\right)_{\mathrm{dB}} = 20\log\left(\frac{\frac{2}{\theta}}{\frac{2}{N\theta}}\right) = 20\log(N)$$

noise degradation in multipliers

- noise transmission matrix
  - Θ → phase mod. AND m → amplitude mod.
  - T → conversion coefficients PM-to-PM, AM-to-PM etc.

$$\begin{pmatrix} \theta_2 \\ m_2 \end{pmatrix} = \begin{pmatrix} T_{\mathrm{pp}} & T_{\mathrm{pa}} \\ T_{\mathrm{ap}} & T_{\mathrm{aa}} \end{pmatrix} \begin{pmatrix} \theta_1 \\ m_1 \end{pmatrix}$$

- ideal multiplier, and good approximation for n = 2

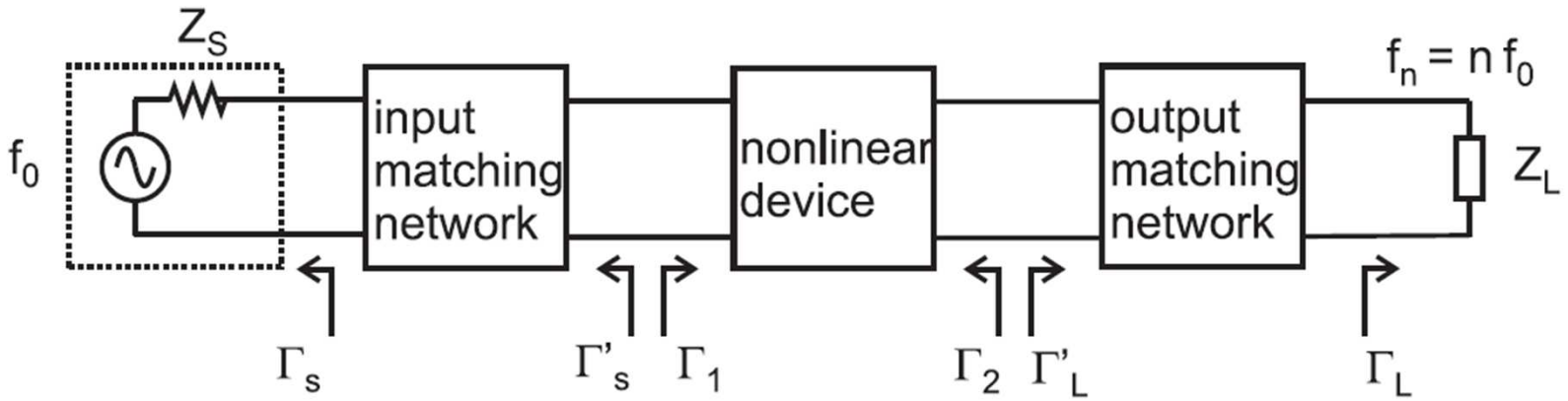
$$T = \begin{pmatrix} n & 0 \\ 0 & 1 \end{pmatrix}$$

- real multiplier, especially for n > 2

$$T = \begin{pmatrix} n & \neq 0 \\ n & 1 \end{pmatrix}$$

harmonic terminations

- input matching network
  - match for fundamental frequency: $\Gamma_{1,0} = \Gamma^*_{s,0}$
  - full reflection of all other harmonics: $\Gamma_{1,i} = \pm 1,\ i \geq 1$
- output matching network
  - match for n-th harmonic: $\Gamma_{2,n} = \Gamma^*_{l,n}$
  - full reflection of all other harmonics: $\Gamma_{2,i} = \pm 1,\ i \mathrel{!}= n$
- idler circuits
  - resonance circuits at intermediate harmonics m = 2..n−1
  - increased conversion efficiency
  - exploit mixing effects for output frequency at harmonic m + n



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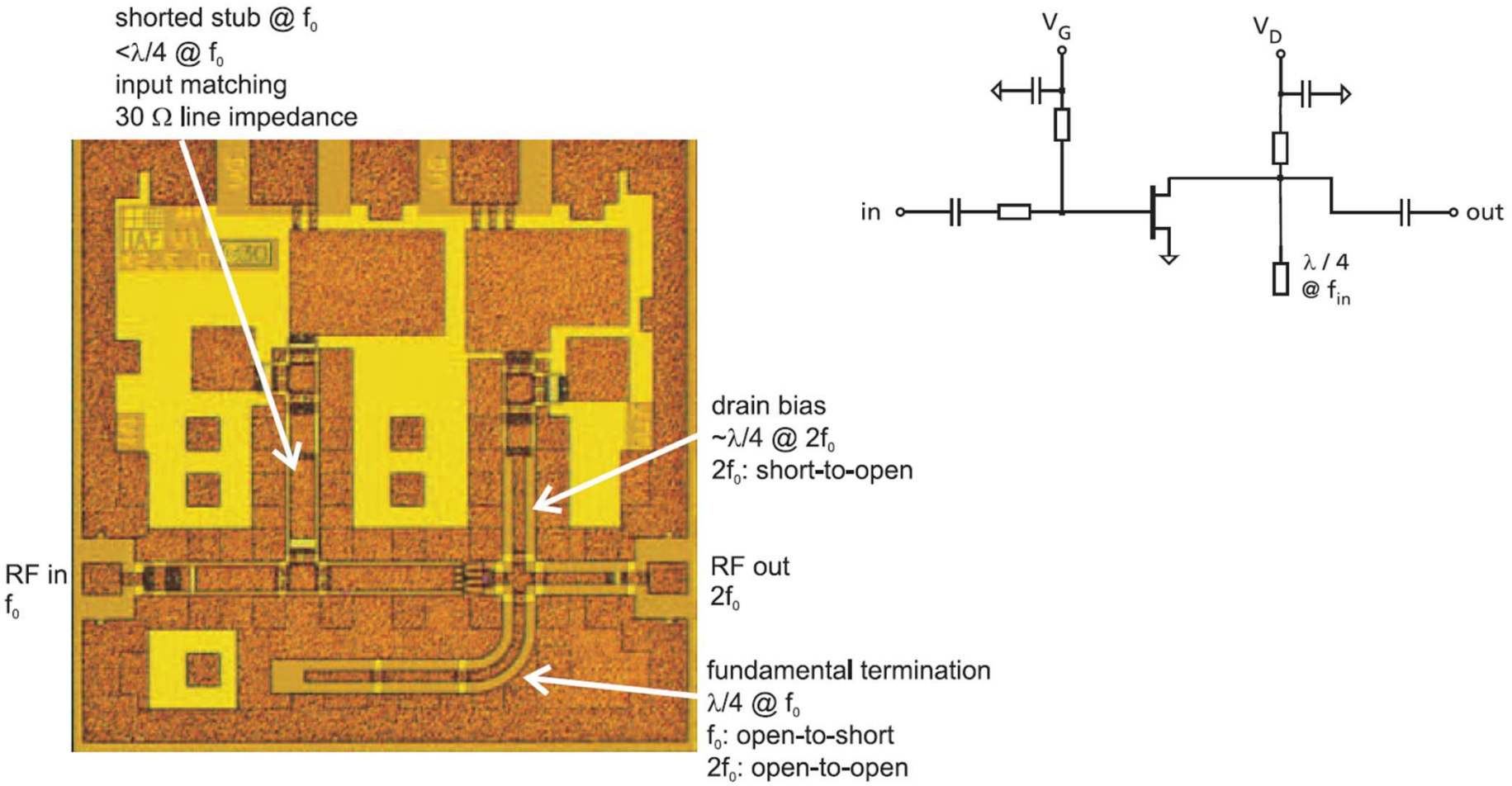
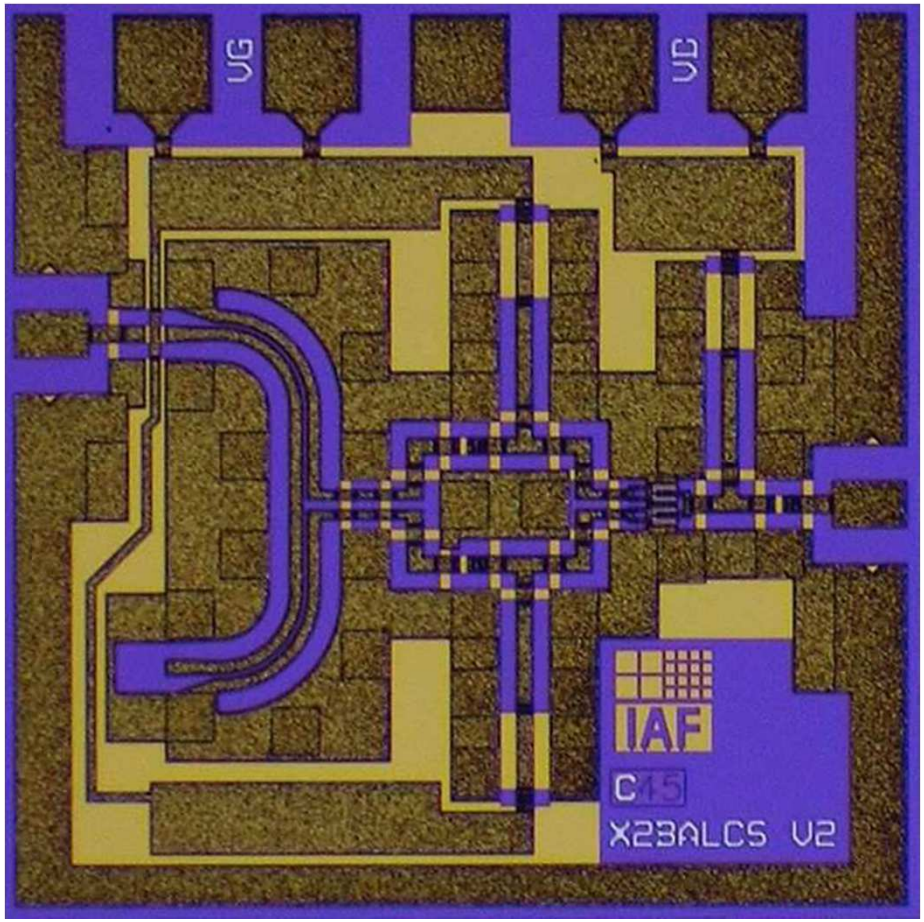
example: single-ended FET doubler

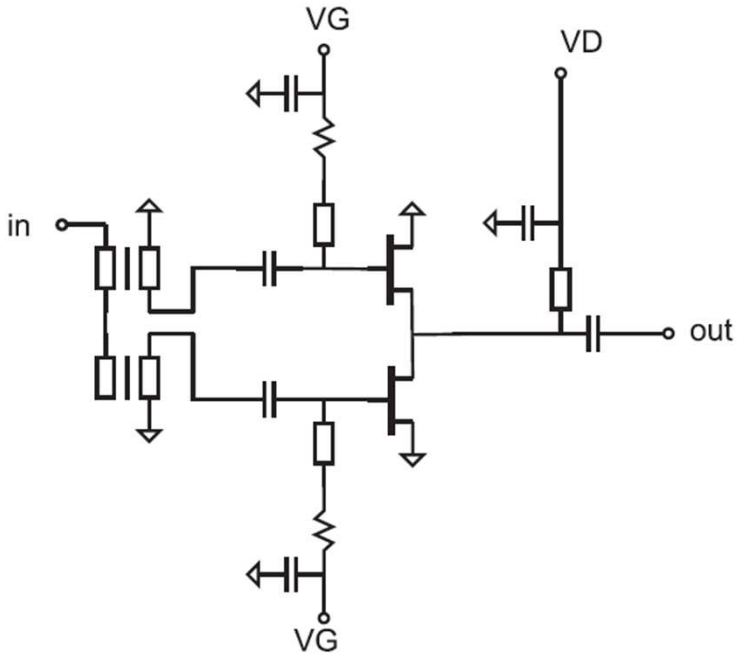
- FET biased under class B conditions ($V_G \approx V_{th}$)
- suppression of f_0 and $N \cdot f_0$ via open ended $\lambda/4$ stub at the output



example: balanced FET doubler

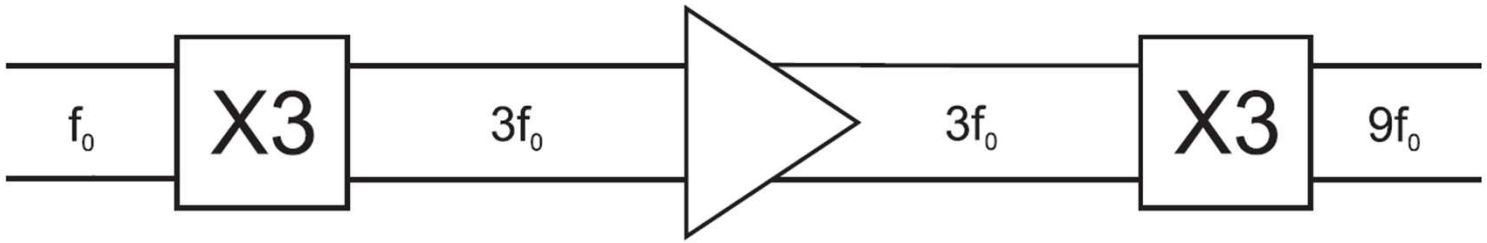
- Marchand UNBAL
- class B FETs





practical example: frequency x9

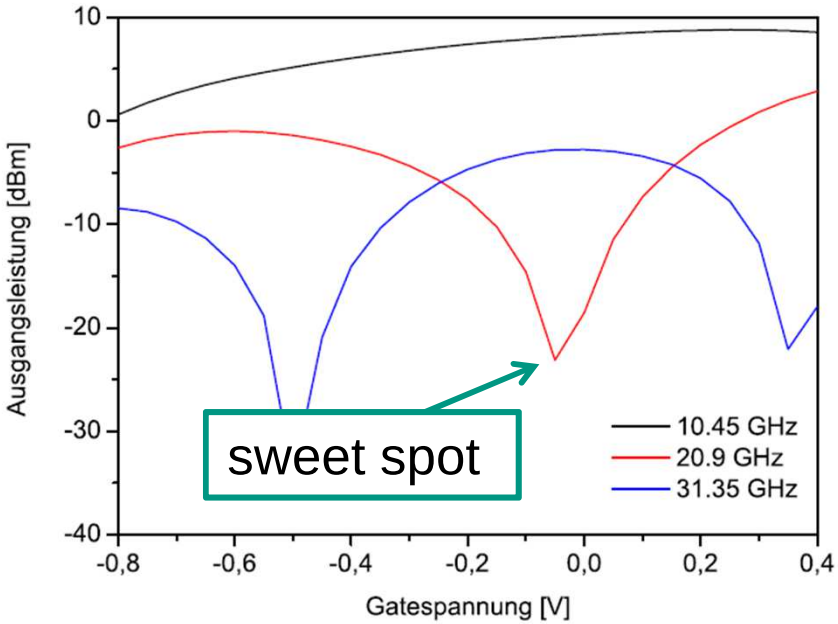
- 100 nm gate-length Fraunhofer IAF mHEMT technology
- signal source in W band (75 to 110 GHz)
  - commercial sources around 10 GHz available
- active frequency multiplication
  - lower conversion losses
  - monolithic integration possible
- FET in CS configuration and driven into compression
  - sinusoidal input → trapezoidal output
  - unwanted harmonics filtered at output

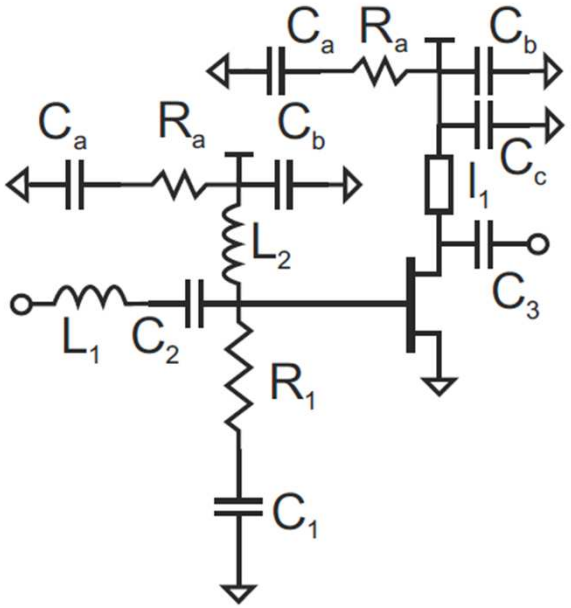


- Source: U. Lewark, „Aktive Frequenzvervielfacher zur Signalerzeugung im Millimeterwellenfrequenzbereich“

practical example: frequency x3

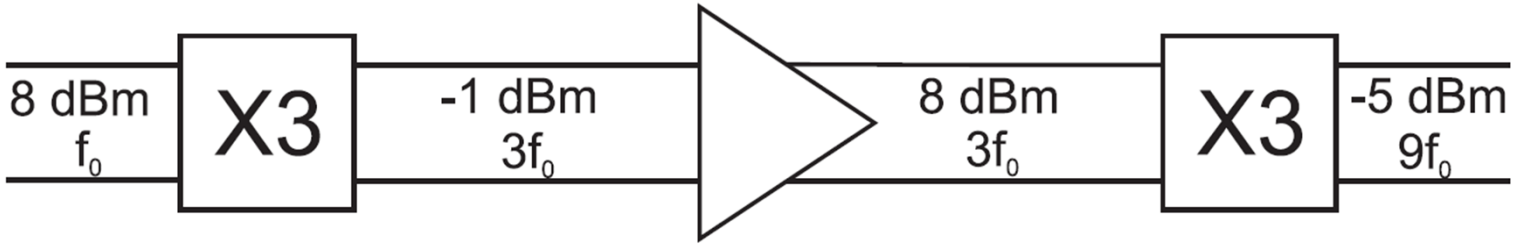
- 2x30 µm FET in CS configuration
- f_0 = 10.45 GHz → 3·f_0 = 31.33 GHz
- P_{in} = 5 dBm → saturation
- sweet spot at class AB biasing
- input matching at f_0 and output matching at 3·f_0 + harmonic suppression

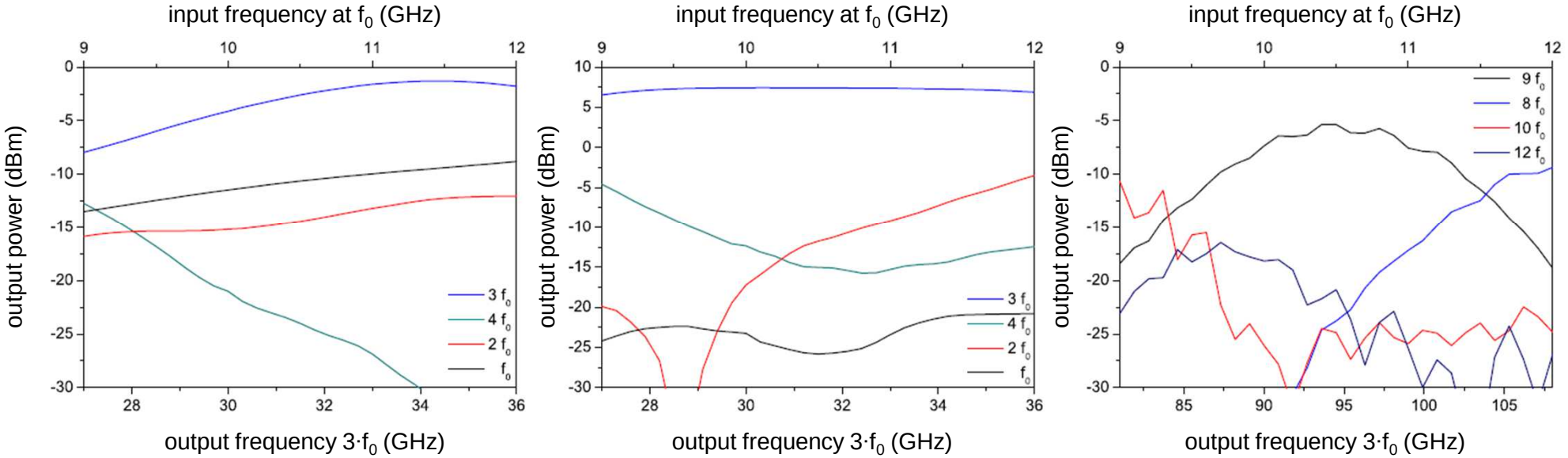




practical example: simulation of overall x9

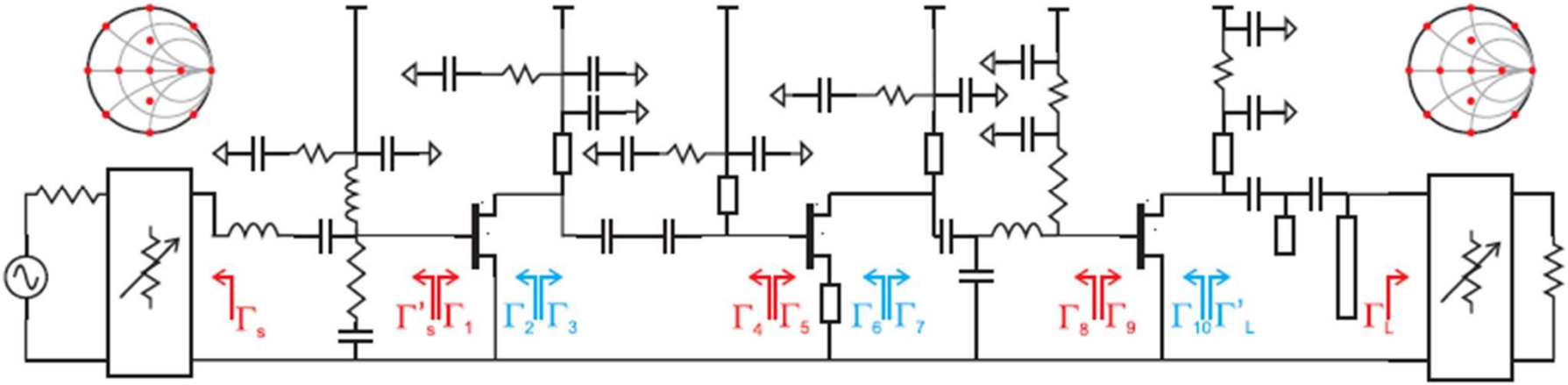
- simulation of power levels
- each stage matched to 50 Ohm → cascading of stages possible
- buffer amplifier improves suppression of unwanted harmonics

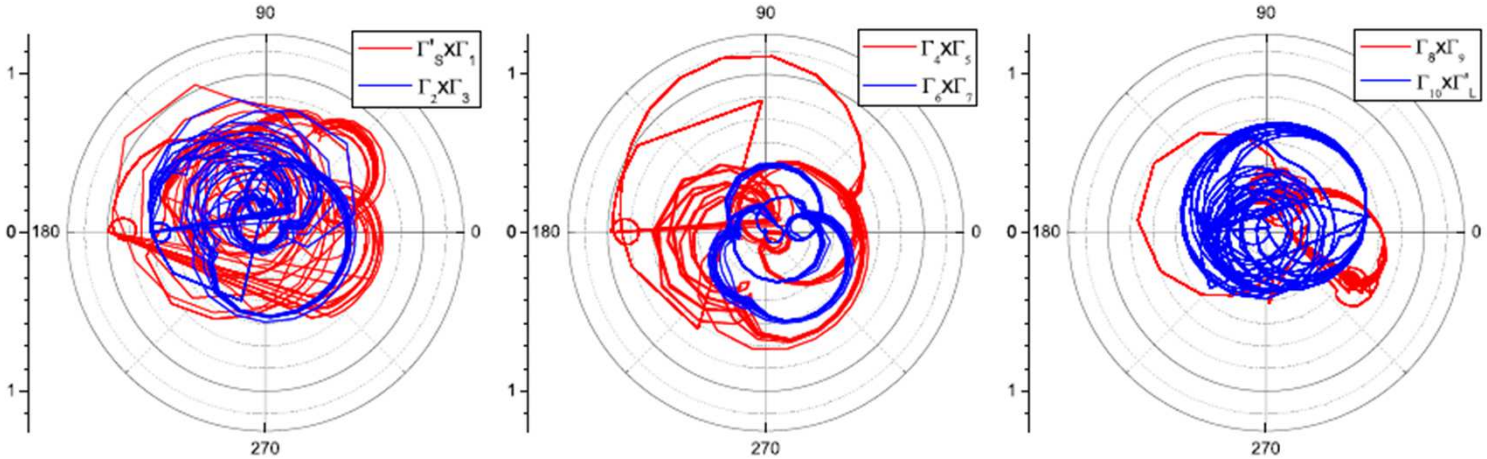




practical example: stability

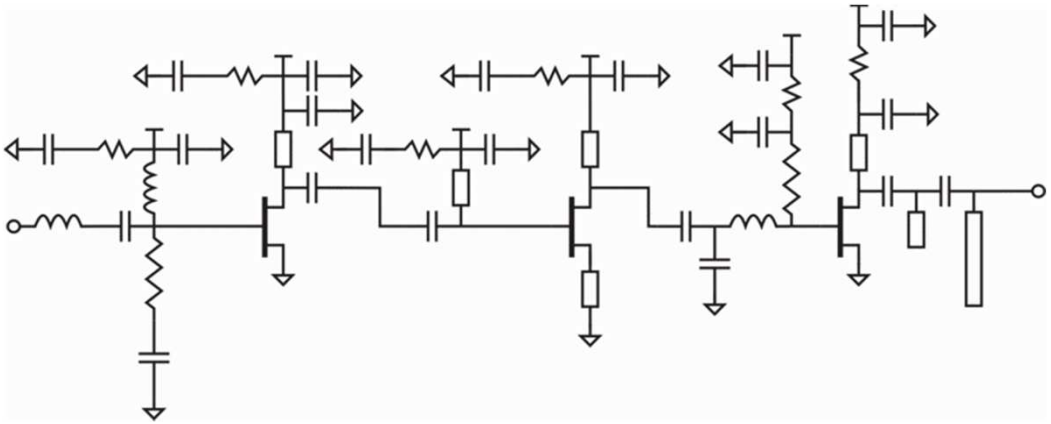
- investigation with Gamma-Probes

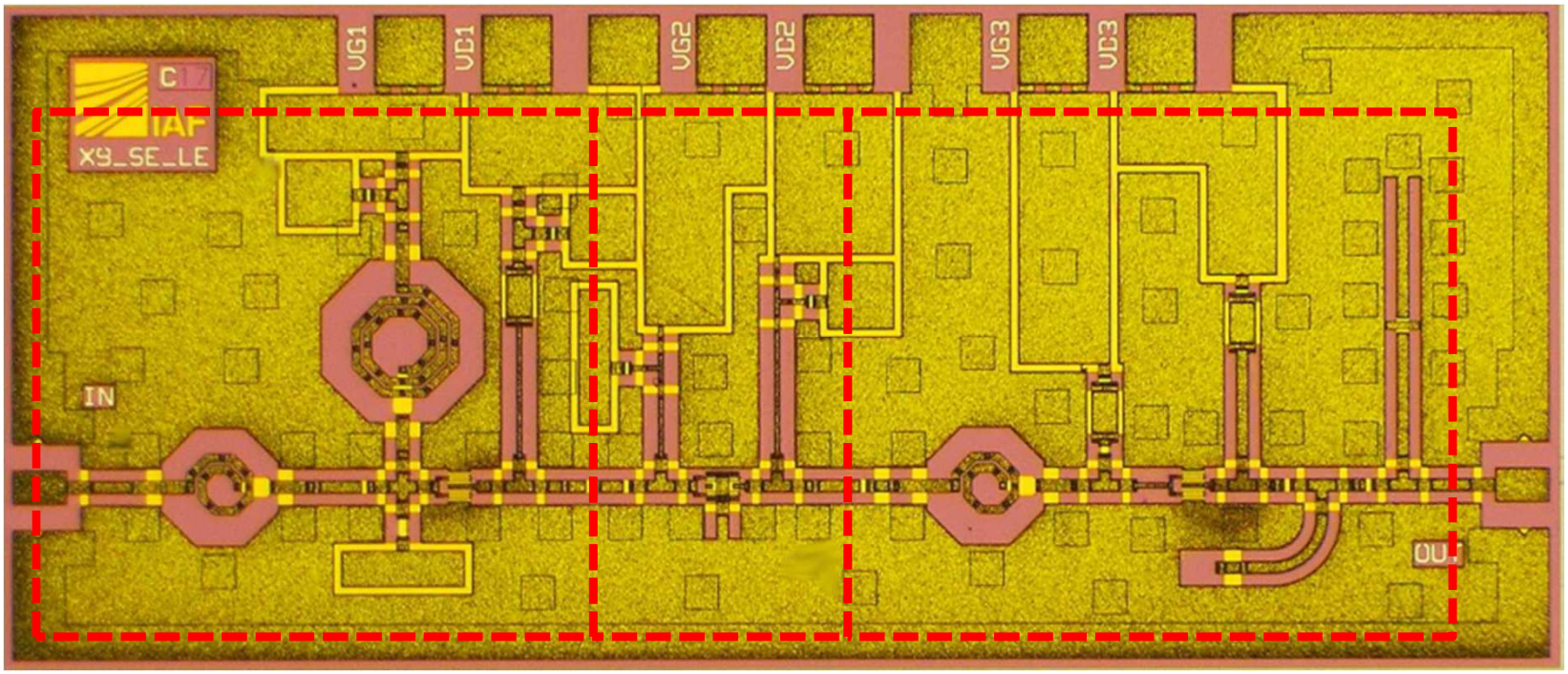




practical example: chip photograph

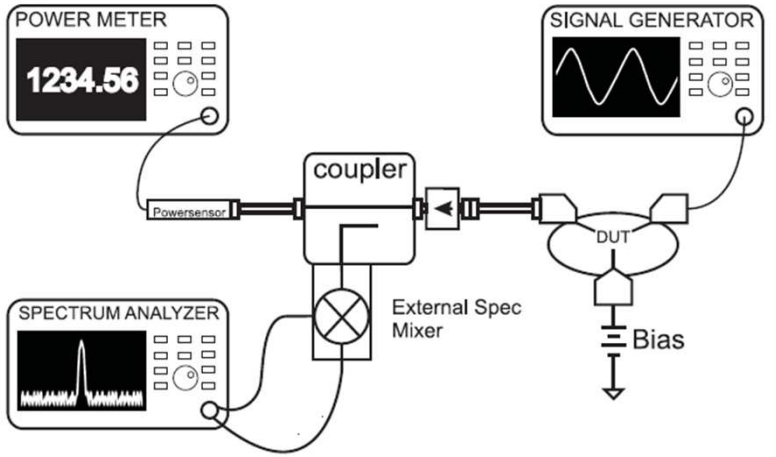
- size: 1 x 2.25 mm^2

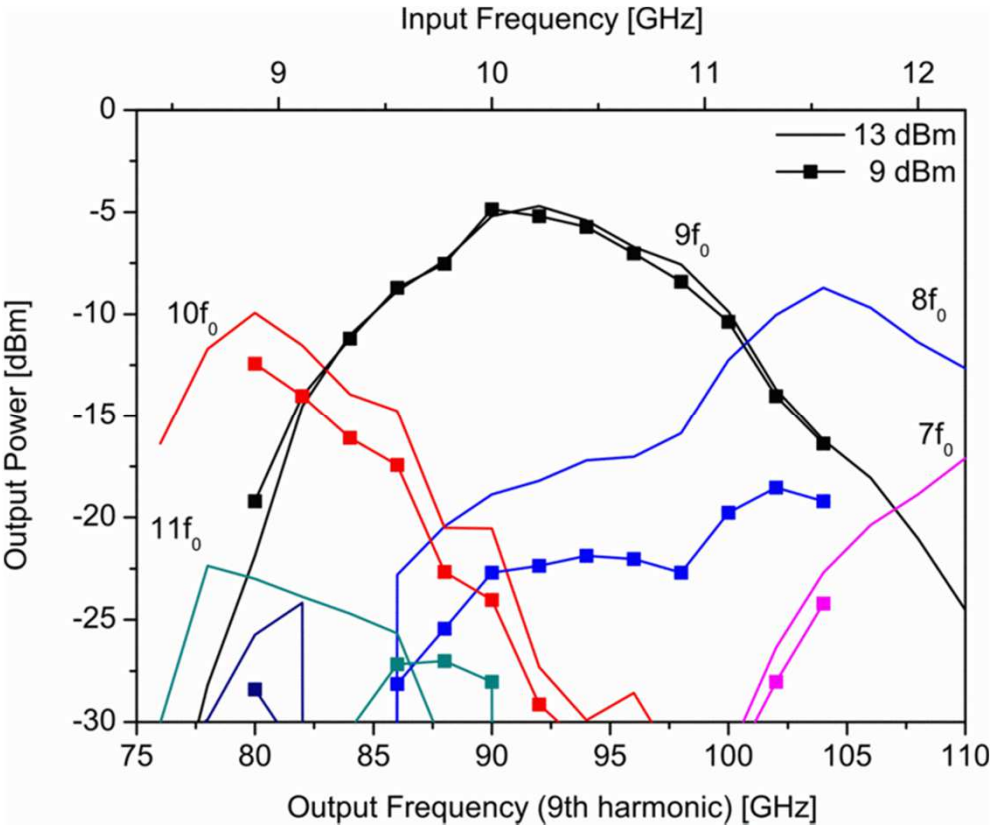


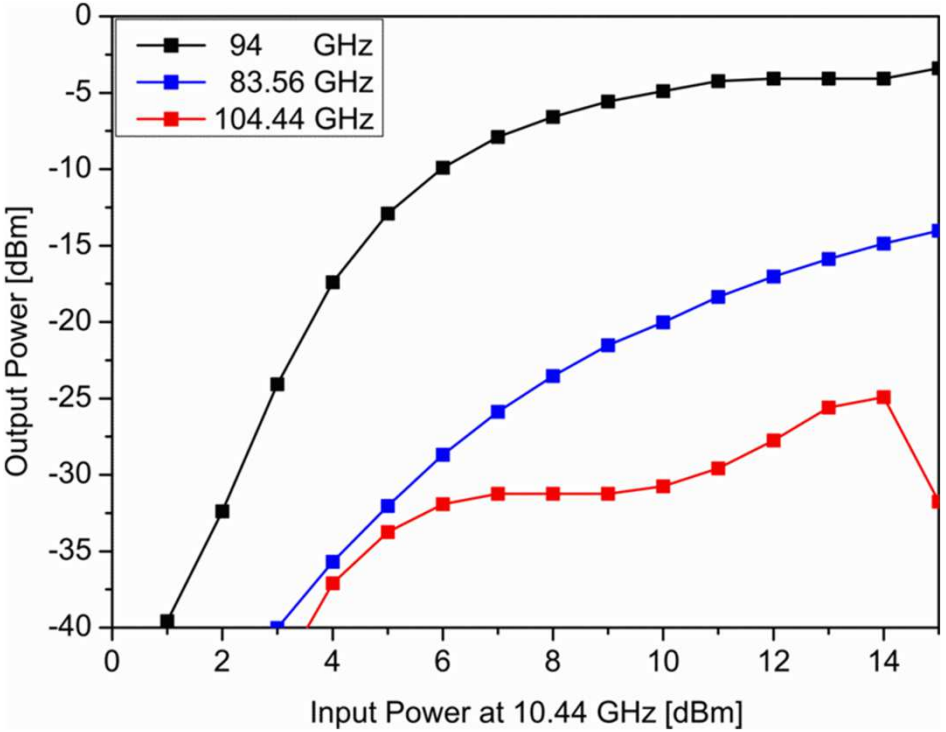


practical example: power meas.

- system calibration for all harmonics
- left: variation of frequency and power
- right: variation of input power







practical example: noise measurement

- theory: noise degradation by 20·log(N)
- reality: noise conversation effect possible
- comparison of curve (a) and (b) show that theory is valid